

PTO-1449 (Modified) 3 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2DC	SERIAL NUMBER 09/545,648
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 10, 2000	GROUP ART UNIT 2781

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	4,445,204	04/24/84	Nishiguchi	—	—	
BA	4,821,226	04/11/89	Christopher et al.	—	—	
BA	4,882,712	11/21/89	Ohno et. al.	—	—	
BA	4,951,251	08/21/90	Yamaguchi et al.	—	—	
BA	4,928,265	5 12/29/90 27	Higuchi et al. Bohne et al.	—	—	
BA	5,107,465	04/21/92	Fung et al.	—	—	

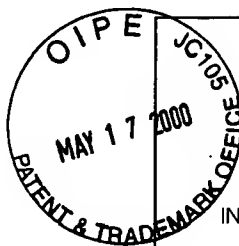
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

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BA i	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
BA 2	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
BA 3	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)

EXAMINER <i>Glen Anne</i>	DATE CONSIDERED <i>9/6/2000</i>
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MS	5 4,206,833	04/27/93	Lee	—	—	
GA	4,953,128	08/28/90	Kawai et al.	—	—	
GA	5,140,688	08/18/92	White et al.	—	—	
GA	5,018,111	05/21/91	Madland	—	—	
GA	4,845,664	07/04/89	Aichelmann, Jr. et al.	—	—	
GA	4,734,880	03/29/88	Collins	—	—	

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✓ GA 4	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5- μ m Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988) ✓
✓ GA 5	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988) ✓
✓ GA 6	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87) ✓
✓ GA 7	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987 ✓
✓ GA 8	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986) ✓
✓ GA 9	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990) ✓
GA 10	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
GA 11	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
GA 12	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990) ✓

EXAMINER G. Kim Anne	DATE CONSIDERED 9/6/2000
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<i>MA</i>	4,183,095	01/08/80	Ward	—	—	
<i>MA</i>	4,975,872	12/04/90	Zaiki	—	—	
<i>MA</i>	5,016,226	05/14/91	Hiwada et al.	—	—	
<i>MA</i>	4,853,896	08/01/89	Yamaguchi	—	—	
<i>MA</i>	4,747,079	05/24/88	Yamaguchi	—	—	
<i>MA</i>	4,945,516	07/31/90	Kashiyama	—	—	

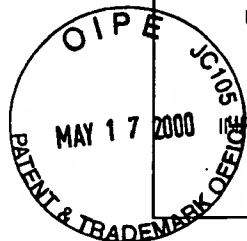
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<i>MA</i> 13	S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982) ✓
<i>MA</i> 14	K. Numata et. al. "New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24, No. 4, pp. 900-904 (Aug. 1989) ✓
<i>MA</i> 15	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990) ✓
<i>MA</i> 16	J. Sonntag et al. "A Monolithic CMOS 10MHz DPLL for Burst-Mode Data Retiming", IEEE International Solid State Circuits Conference (ISSCC) February 16, 1990

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>JA</i>	4,649,511	03/10/87	Gdula	—	—	
<i>JA</i>	4,860,198	08/22/89	Takenaka	—	—	
<i>JA</i>	3,969,706	07/13/76	Proebsting et al.	—	—	
<i>JA</i>	4,766,536	08/23/88	Wilson, Jr. et al.	—	—	
<i>JA</i>	4,998,262	03/05/91	Wiggers	—	—	
<i>JA</i>	4,757,473	07/12/88	Kurihara et al.	—	—	
<i>JA</i>	4,792,926	12/20/88	Roberts	—	—	
<i>JA</i>	4,811,202	03/07/89	Schabowski	—	—	
<i>JA</i>	5,034,917	07/23/91	Bland et al.	—	—	
<i>JA</i>	5,301,278	04/05/94	Bowater et al.	—	—	
<i>JA</i>	5,153,856	10/06/92	Takahashi	—	—	
<i>JA</i>	4,845,670	07/04/89	Nishimoto et al.	—	—	

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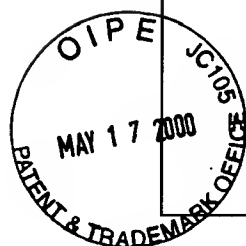
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>JA</i>	0 276 871 ✓	03/08/88	DE FR GB IT EPX	—	—	

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✓ <i>JA 17</i>	M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987) ✓
✓ <i>JA 18</i>	R. L. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Coding Applications", IEEE Transactions on Circuits And Systems, vol. 36 No. 10, pp. 1275-1280 (Oct 1989) ✓
✓ <i>JA 19</i>	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. SC-18 No. 5, pp. 561-567 (Oct. 1983) ✓
✓ <i>JA 20</i>	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989) ✓

EXAMINER Glenn Anne	DATE CONSIDERED 9/6/2000
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	4,685,088	08/04/87	Iannucci	<i>1</i>	<i>1</i>	
<i>MA</i>	4,509,142	04/02/85	Childers	<i>1</i>	<i>1</i>	
<i>MA</i>	5,051,889	09/24/91	Fung et al.	<i>1</i>	<i>1</i>	
<i>MA</i>	5,361,277	11/01/94	Grover	<i>1</i>	<i>1</i>	
<i>MA</i>	4,954,987	09/04/90	Auvinen et al.	<i>1</i>	<i>1</i>	
<i>MA</i>	4,570,220	02/11/86	Tetrick et al.	<i>1</i>	<i>1</i>	
<i>MA</i>	4,247,817	01/27/81	Heller	<i>1</i>	<i>1</i>	
<i>MA</i>	4,519,034	05/21/85	Smith et al.	<i>1</i>	<i>1</i>	
<i>MA</i>	3,691,534	09/12/72	Varadi et al.	<i>1</i>	<i>1</i>	
<i>MA</i>	4,920,486	04/24/90	Nielsen	<i>1</i>	<i>1</i>	
<i>MA</i>	4,263,650	04/21/81	Bennett et al.	<i>1</i>	<i>1</i>	

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<i>MA</i>	0 276 871	03/08/88	<i>dup, DE FR GB IT EPX</i>	<i>1</i>	<i>1</i>	

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<i>MA 22</i>	J. Peterson, "System-Level Concerns Set Performance Gains", High Performance Systems, pp. 71-77 (Sept. 89)	✓
<i>MA 23</i>	N. Margulis, "Single Chip CPU Eases Single Chip System Design", High Performance Systems, pp. 34-44 (Sept. 89)	✓
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<i>MA 25</i>	D.T. Wong, "An 11-ns 8Kx18 CMOS Static RAM with 0.5-um Devices", IEEE Journal of Solid State Circuits, vol. 23, No. 5, pp. 1095-1103 (Oct. 1988)	✓
<i>MA 26</i>	A. Agarwal et al., "An Evaluation of Directory Schemes for Cache Coherence", IEEE, pp. 280-289, 1988	✓

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<i>MA</i>	5,023,488	06/11/91	Gunning	—	—	
<i>MA</i>	4,754,433	06/28/88	Chin et al.	—	—	
<i>MA</i>	3,771,145	11/06/73	Wiener	—	—	
<i>MA</i>	5,021,985	06/04/91	Hu et al.	—	—	

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<i>MA 27</i>	T. L. Jeremiah, "SYNCHRONOUS LSSD PACKET SWITCHING MEMORY AND I/O CHANNEL", IBM Technical Bulletin vol. 24 No. 10, pp. 4986-4987 (March 1982)
<i>MA 28</i>	D. Hawley, "Superfast Bus Supports Sophisticated Transactions", High Performance Systems, pp. 90-94 (Sept. 89)
<i>MA 29</i>	M. Bazes, "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. SC-18, No. 2, pp. 164-172 (April 1983)
<i>MA 30</i>	D. Wendell et al., "A 3.5ns Self Timed SRAM", IEEE 1990 Symposium on VLSI Circuits pp. 49-50 ✓
<i>MA 31</i>	J. Chun et al., "A pipelined 650 MHz GaAs 8K ROM with Translation Logic" IEEE 1990 GaAs IC Symposium, pp 139-142
<i>MA 32</i>	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989) ✓

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✓ MA 33	European Search Report for EPO Patent Application No. 00 10 0018
✓ MA 34	European Search Report for EPO Patent Application No. 00 10 822

EXAMINER <i>Glynn Anne</i>	DATE CONSIDERED <i>7/6/2000</i>
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OA	S57-14922	Jan. 26, 1982	Japan	—	—	YES	
OA	Sho 60-80193	May 8, 1983	Japan	—	—	YES	
OA	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES	
OA	S61-72350	April 14, 1986	Japan	—	—	YES	
OA	S63-142445	June 14, 1988	Japan	—	—	YES	
OA	B63-46864	Sept. 19, 1988	Japan	—	—	YES	
OA	S64-29951	Jan. 31, 1989	Japan	—	—	YES	

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OA	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
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OA	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
OA	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
OA	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

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MA	4,845,670	Jul. 4, 1989	Nishimoto et al. D28	—	—	
PA	4,509,142	Apr. 2, 1985	Childers D28	—	—	
MA	4,183,095	Jan. 8, 1980	Ward D28	—	—	
MA	4,685,088	Aug. 4, 1987	Ianucci D28	—	—	

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MA	0 334 552	Mar. 16, 1989	EPO	—	—	
MA	0 276 871	Jan. 29, 1988	EPO	—	—	

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MA	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
MA	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
MA	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
MA	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
MA	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
MA	JEDEC Standard No. 21C

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